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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 18

Application Number: 09/606,057
Filing Date: June 28, 2000
Appellant(s): CHAUVEL ET AL.

Ronald O. Neerings
For Appellant

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Technology Center 2100

EXAMINER'S ANSWER

This is in response to the appeal brief filed 12/27/02.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 6, 8, 10, 13-14, 16-17, and 19 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

6,282,180	Paneth et al.	8-2001
4,829,554	Barnes et al.	5-1989

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 6, 8, 10, 13-14, 16-17, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Paneth et al., U.S. Patent No. 6,282, 180 B1, (hereinafter Paneth), and further in view of Barnes et al., U.S. Patent No. 4,829, 554, (hereinafter Barnes).

As per claim 6, Paneth teaches the invention substantially as claimed, a radio, comprising: a first processor being the main processor of the radio (e.g., fig.2, el. 24 or 18 or 20 or fig.3, el. 27 or el. 28 or 29; and col. 8, line 54 and et seq.); a second processor coupled to the first processor wherein said second processor performs protocol processing (e.g., fig.2, el.18 or fig.3, el. 29; and col. 8, lines 22-24); a third processor coupled to the first processor wherein the third processor performs signal processing on vectors processing (e.g., fig.3, el. 33 or 30a or fig. 25, el. 154; col. 71, line 64 and et seq.). Paneth does not explicitly show the use of cellular. Barnes, e.g., abstract, lines 1-4, is shown as an example that a cellular radio being well known in the art. It would have been obvious to one of ordinary skill in the art at the time the

invention was made to have a cellular radio to the system of Paneth because it would allow distribution of many of the control functions to cell stations associated with cells; thereby, monitoring and voice communication functions provides both security from interrupted service and significant reduced costs.

As per claim 8, 10, 13, and 16, Paneth teaches wherein said first processor performs management and vocoder signal processing (e.g., fig.2, el. 24 or 17 or 20 or fig.3, el. 28 or 29; col. 7, line 63 and et seq. or col. 41, line 31); wherein the second processor is a dedicated processor adapted to bit processing (e.g., fig.2, el. 24 or 16 or 18 or 20 or fig.3, el. 27 or 28 or 29 or fig. 25, el. 154; col. 17, line 40 and et seq.); wherein the three processors operate in parallel (e.g., abstract, line 1 and et seq.); and wherein the first processor is a DSP (e.g., col. 42, lines 53-60).

As per claim 14, Paneth teaches the invention substantially as claimed, a radio, comprising: a first processor performing management and vocoder signal processing (e.g., fig.2, el. 24 or 17 or 20 or fig.3, el. 28 or 29; col. 7, line 63 and et seq. or col. 41, line 31); a second processor coupled to the first processor wherein said second processor performs protocol processing (e.g., fig.2, el.18 or fig.3, el. 29; and col. 8, lines 22-24); a third processor coupled to the first processor wherein the third processor performs signal processing on vectors (e.g., fig.3, el. 33 or 30a or fig. 25, el. 154; col. 71, line 64 and et seq.). Paneth does not explicitly show the use of cellular. Barnes, e.g., abstract, lines 1-4, is shown as an example that a cellular radio being well known in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a cellular radio to the system of Paneth because it would

allow distribution of many of the control functions to cell stations associated with cells; thereby, monitoring and voice communication functions provides both security from interrupted service and significant reduced costs.

As per claims 17 and 19, Paneth teaches wherein the first processor is a DSP (e.g., col. 42, lines 53-60); wherein the second processor is a dedicated processor adapted to bit processing (e.g., fig.2, el. 24 or 16 or 18 or 20 or fig.3, el. 27 or 28 or 29 or fig. 25, el. 154; col. 17, line 40 and et seq.).

3. Claim 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Paneth et al., U.S. Patent No. 6,282, 180 B1, (hereinafter Paneth), and in view of Barnes et al., U.S. Patent No. 4,829, 554, (hereinafter Barnes), and further in view of Claesson et al., a Multi-DSP implementation of a Broad-Band Adaptive Beamformer for Use in a Hands-Free Mobile Radio Telephone, pages 194-200, 02/1991 (hereinafter Claesson).

As per claim 16, Paneth teaches the first processor being the main processor of the radio (e.g., fig.2, el. 24 or 18 or 20 or fig.3, el. 27 or 29; and col. 8, line 54 and et seq.). Paneth does not explicitly show the above processor being a DSP. Claesson shows the use of a DSP (e.g., col. 2, page 194 to col. 1, page 195) in a radio system. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Claesson into the combines system of Paneth and Barnes because it would allow a highest performance, available in various forms and performance levels from all major semiconductor manufacturers, increase execution

speed and keep the cost reasonable, as taught by Claesson(e.g., col. 2, page 194 to col. 1, page 195).

As per claim 17, Paneth teaches the first processor performing management and vocoder signal processing (e.g., fig.2, el. 24 or 20 or fig.3, el. 29 ; col. 7, line 63 and et seq. or col. 41, line 31). Paneth does not explicitly show the above processor being a DSP. Claesson shows the use of a DSP (e.g., col. 2, page 194 to col. 1, page 195) in a radio system. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Claesson into the combines system of Paneth and Barnes because it would allow a highest performance, available in various forms and performance levels from all major semiconductor manufacturers, increase execution speed and keep the cost reasonable, as taught by Claesson(e.g., col. 2, page 194 to col. 1, page 195).

4. Claim 12, 15, 18, and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Paneth et al., U.S. Patent No. 6,282, 180 B1, (hereinafter Paneth), in view of Barnes et al., U.S. Patent No. 4,829, 554, (hereinafter Barnes), and further in view of Mano, Computer System Architecture, Prentice-Hall Inc., pages 282-284, 1982 (hereinafter Mano).

As per claims 12 and 21, Paneth does not explicitly show the use of an array processor. Mano as an example shows that both the concept and advantages of having a processor being an array processor are well known and expected in the art (page 282). It would have been obvious to one of ordinary skill in the art at the time the

invention was made to combine Mano with the combined system of Paneth and Barnes because it would provide for parallel computations on large arrays, thereby increasing system computation power.

As per claim 15, Paneth teaches the invention substantially as claimed, a radio, comprising: a first processor performing management and vocoder signal processing (e.g., fig.2, el. 24 or 17 or 20 or fig.3, el. 28 or 29 ; col. 7, line 63 and et seq. or col. 41, line 31); a second processor coupled to the first processor wherein said second processor performs protocol processing (e.g., fig.2, el.18 or fig.3, el. 29; and col. 8, lines 22-24); a third processor coupled to the first processor wherein the third processor performs signal processing (e.g., fig.3, el. 33 or 30a or fig. 25, el. 154; col. 71, line 64 and et seq.). Paneth does not explicitly show the use of cellular. Barnes, e.g., abstract, lines 1-4, is shown as an example that a cellular radio being well known in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a cellular radio to the system of Paneth because it would allow distribution of many of the control functions to cell stations associated with cells; thereby, monitoring and voice communication functions provides both security from interrupted service and significant reduced costs. Paneth does not explicitly show the use of an array processor. Mano as an example shows that both the concept and advantages of having a processor being an array processor are well known and expected in the art (page 282). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Mano with the combined system

of Paneth and Barnes because it would provide for parallel computations on large arrays, thereby increasing system computation power.

As per claims 18 and 20, Paneth teaches wherein the first processor is a DSP (e.g., col. 42, lines 53-60); wherein the second processor is a dedicated processor adapted to bit processing (e.g., fig.2, el. 24 or 16 or 18 or 20 or fig.3, el. 27 or 28 or 29 or fig. 25, el. 154; col. 17, line 40 and et seq.).

5. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Paneth et al., U.S. Patent No. 6,282, 180 B1, (hereinafter Paneth), in view of Barnes et al., U.S. Patent No. 4,829, 554, (hereinafter Barnes), further in view of Mano, Computer System Architecture, Prentice-Hall Inc., pages 282-284, 1982 (hereinafter Mano), and further in view of Claesson.

As per claim 18, Paneth teaches the first processor performing management and vocoder signal processing (e.g., fig.2, el. 24 or 20 or fig.3, el. 29 ; col. 7, line 63 and et seq. or col. 41, line 31). Paneth does not explicitly show the above processor being a DSP. Claesson shows the use of a DSP (e.g., col. 2, page 194 to col. 1, page 195) in a radio system. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Claesson into the combines system of Paneth and Barnes because it would allow a highest performance, available in various forms and performance levels from all major semiconductor manufacturers, increase execution speed and keep the cost reasonable, as taught by Claesson(e.g., col. 2, page 194 to col. 1, page 195).

(11) Response to Argument

Applicant's arguments filed 12/27/02 have been fully considered but they are not persuasive.

1. In the Appellant's Argument, the appellant argued (1) that Paneth fails to suggest that processor 20 is the main processor of the base station or of any cellular radio as required by claim 6.

In response to the appellant's argument (1), The combination of Paneth and Barnes teaches the first processor being main processor of a cellular radio as stated above in the rejection with respect to claim 6. In particular, Paneth teaches that processor 20 is the main processor of the base station (e.g., col. 8, line 54 and et seq.).

2. In the Appellant's Argument, the appellant argued (2) that "Paneth discloses nothing more than that "the remote control processor unit (RPU) 20 is the central control processor . . . Paneth does not teach or suggest that RPU 20 is the main processor of a cellular', as required by claim 6 . . . the combination of Paneth and Barnes is not the prior art. . ." (Appellant's Brief received 27/12/02. page 13, "response to Examiner's rebuttal (9)"

In response to appellant's argument (2) that according to col. 8, lines 54-63, Paneth teaches the processor 20 is not only the central control (i.e., dominant control or most control) processor but also the most important control processor because it

performs the system management functions, controls the other elements, such as processor 18 (col. 8, lines 23-25), modem 19, RFU 21 (col. 8, lines 44-47), control mechanisms for call set up, teardown, and maintenance, and control the interconnection between codecs 16 and the Telco trunks. Therefore, Paneth teaches the processor is the main processor of the base or the radio. In addition, Paneth teaches the processor 20 is the main processor because it is located on a base station (e.g., figs. 1-2, the base station and processor 20) which is the first important (i.e., primary) station (abstract line 1) and is the most control station for controlling the other stations (col. 7, lines 20-25).

Paneth does not explicitly show the use of cellular. Barnes, e.g., abstract, lines 1-4, is shown as an example that a cellular radio being well known in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a cellular radio to the system of Paneth because it would allow distribution of many of the control functions to cell stations associated with cells; thereby, monitoring and voice communication functions provides both security from interrupted service and significant reduced costs.

The combination of Paneth and Barns is the prior art because the rejections based on the combination of Paneth and Barns but not based on Paneth individually or Barnes individually. Therefore, The Examiner's statement "The combination of Paneth and Barnes teaches the first processor being main processor of a cellular radio as stated above in the rejection with respect to claim 6" as stated above is respectfully maintained.

3. In the Appellant's Argument, the appellant argued (3) nowhere is in Paneth teaches or suggest that STU 27 is a processor or main processor of the cellular radio (Appellant's Brief received 12/27/02. pages 16, lines 5-8).

In response to the applicant's arguments (3), The combination of Paneth and Barnes teaches the first processor being main processor of a cellular radio as stated above in the rejection with respect to claim 6. In particular, col. 41, lines 31-44 and fig. 3, el. 27 and fig. 12, Paneth teaches that the element 27 is a processor (i.e., one that processes, comprising the micropro controller 58 (fig. 12) and converting voice signal).

In further discussion, according to col. 9, lines 10-13, Paneth teaches the processor 27 is the most important control processor (i.e. main) because it performs all control functions of the subscriber or the radio.

In addition, Paneth does not explicitly show the use of cellular. Barnes, e.g., abstract, lines 1-4, is shown as an example that a cellular radio being well known in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a cellular radio to the system of Paneth because it would allow distribution of many of the control functions to cell stations associated with cells; thereby, monitoring and voice communication functions provides both security from interrupted service and significant reduced costs.

4. In the Appellant's argument, the appellant argued (4) that Paneth fails to suggest wherein the first processor performs management and vocoder signal processing as

required by claims 14 and 15. Also, the vocoder function is performed by the codecs in VCU 17 not in RPU 20.

In response to the appellant 's arguments (4), Paneth teaches a first processor performing management and vocoder signal processing (e.g., fig.2, el. 24 or 17 or 20 or fig.3, el. 28 or 29 ; col. 7, line 63 and et seq. or col. 41, line 31). For example, Paneth teaches main processor 20 performing management and vocoder signal processing by controlling the performance vocoder signal processing, the interconnections between the codecs 16 (e.g., col. 8, lines 56-63).

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the vocoder function is performed by the codecs in VCU 17 not in RPU 20) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

5. In the Appellant's Argument, the appellant argued (5) nowhere in Paneth that teaches any one of the call processor 24, voice codec unit 17, remote connection processor 20, voice codec unit 28, or channel control unit 29 is "a processor that 'performs management and vocoder signal processing' as required by claim 14" (Appellant's Brief received 12/27/02. pages 13-14, "response to Examiner's rebuttal (10)"

6. In the Appellant's Argument, the appellant argued (6) nowhere in Paneth teaches that el. 27 and el. 28 are processors which perform management and vocoder signal processing as required by claim 14 (Appellant's Brief received 12/27/02. page 18, first paragraph.

In response to appellant's arguments (5) and (6), as stated in the previous office actions Paneth teaches the processor 20 performs management and vocoder signal processing by controlling the vocoder signal processing, the interconnections between the codecs 16 (e.g., col. 8, lines 56-63).

According to col. 7, lines 60-67 and fig. 2, Paneth teaches the processor 15 (i.e., one that processes, comprising the processor 24 and converting voice information to pulse code modulation) performs management (e.g., col. 7, lines 61-63; col. 8, lines 6-64) and vocoder signal processing (e.g., col. 7, lines 63-67).

In addition, col. 41, lines 31-44 and fig. 3, el. 27 and fig. 12, Paneth teaches the processor 27 (i.e., one that processes, comprising the micropro controller 58 (fig. 12) and converting voice signal) performs management (e.g., col. 42, lines 33-40) and vocoder signal processing (e.g., col. 41, lines 30-35).

Further more, Paneth teaches the CCU processor 29 (i.e., one that processes, comprising the microprocessor 111 (fig. 21) and converting voice signal) performs management (e.g., col. 49, line 59 to col. 50, line7; col. 51, lines 29-32) and vocoder signal processing (e.g., col. 49, lines 28-60; col. 53, lines 45-50).

Paneth teaches the Voice Codec unit 28 is the processor (e.g., col. 42, lines 50-60) performs management (e.g., col. 46, lines 60 to col. 65) and vocoder signal processing (e.g., col. 8, lines 5-15).

7. In the Appellant's Argument, the appellant argued (7) that "just because 'RPU 20 . . . control the interconnections between the codes 6 and the Telcon trunks accomplished by a switch matrix 25 of the PBX', does not mean that RPU performs vocoder signal processing", as required by claim 14 (Appellant's Brief received 12/27/02. page 14, "response to Examiner's rebuttal (10)"

In response to appellant's argument (7), vocoder signal processing is not only performed by the codecs in VCU 17 but also, by the other elements in the radio, such as the processor 20. The processor 20 control which voice call to be processed by which codecs (e.g., col. 8, lines 54-65; lines 4-20) means perform vocoder signal processing.

8. In the Appellant's Argument, the appellant argued (8) with respect to claims 6, 14, and 15 that the Examiner's combination of Paneth and Barnes is not The Prior Art (Appellant's Brief received 12/27/02. pages 14-17, "response to Examiner's rebuttal (11), (12), "

In response to appellant's argument that (8) the combination of Paneth and Barns is the prior art because the rejections based on the combination of Paneth and Barns but not based on Paneth individually or Barnes individually. Therefore, The

Examiner's statement "The combination of Paneth and Barnes teaches the first processor being main processor of a cellular radio as stated above in the rejection with respect to claim 6" as stated above is respectfully maintained.

9. In the Appellant's Argument , the appellant argued (9) that Paneth 's fig. 3 fails to teach the main processor of the cellular radio; the second processor performing protocol processing; the third processor performing signal processor on vectors as required by claim 6.

In response to applicant's arguments (9) against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). For this case, the combination of Paneth and Barnes teach the main processor of the cellular radio; the second processor performing protocol processor; the third processor performing signal processor on vectors as stated above in the rejection with respect to claim 6.

For example, in the broadest interpretation of the claim, el. 27, fig. 3 of Paneth reads on the main processor limitation of the claim; el. 29, fig. 3 of Paneth reads on the processor performing protocol processing limitation of the claim; and fig.3, el. 33 or 30a or fig. 25, el. 154; col. 71, line 64 and et seq. reads on the processor performing signal processor on vectors limitation of the claim.

10. In the Appellant's Argument, the appellant argued (10) that Paneth 's fig. 3 fails to teach a cellular radio, comprising: a first processor for performing management and vocoder signal processing; the second processor performing protocol processing; the third processor performing signal processor on vectors as required by claim 14.

In response to appellant' s arguments (10) against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). For this case, the combination of Paneth and Barnes teach the main processor of the cellular radio; the second processor performing protocol processor; the third processor performing signal processor on vectors as stated above in the rejection with respect to claim 14.

For example, in the broadest interpretation of the claim, el. 27 or 28 fig. 3 and col. 41, line 31 and et seq. of Paneth reads on the processor performing management and vocoder signal processing limitation of the claim; el. 29, fig. 3 of Paneth reads on the processor performing protocol processing limitation of the claim; and fig.3, el. 33 or 30a or fig. 25, el. 154; col. 71, line 64 and et seq. of Paneth reads on the processor performing signal processor on vectors limitation of the claim.

11. In the Appellant's Argument, the appellant argued (11) that Paneth 's fig. 3 fails to teach a cellular radio, comprising: a first processor for performing management and

vocoder signal processing; the second processor performing protocol processing; the third processor being a dedicated processor of the array type as required by claim 15.

In response to appellant 's arguments (11) against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). For this case, the combination of Paneth, Barnes, and Mano teach the main processor of the cellular radio; the second processor performing protocol processor; the third processor performing signal processor on vectors as stated above the rejection with respect to claim 15.

For example, in the broadest interpretation of the claim, el. 27 or 28 fig. 3 and col. 41, line 31 and et seq. of Paneth reads on the processor performing management and vocoder signal processing limitation of the claim; el. 29, fig. 3 of Paneth reads on the processor performing protocol processing limitation of the claim; and the combination of Paneth, Barnes, and Mano reads on the processor being a dedicated processor of the array type limitation of the claim as stated above the rejection with respect to claim 15.

12. Appellant's Argument, the appellant argued (12) that Barnes discloses a cellular mobile telephone system not just a cellular radio.

In response to appellant 's arguments (12) against the references individually, one cannot show nonobviousness by attacking references individually where the

rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In response to applicant's argument, the combination of Paneth and Barnes teach a cellular radio as stated above. Also, the examiner fails to see why the applicant said that Barnes disclosed a cellular mobile telephone system not just a cellular radio. Barnes teaches a cellular radio (e.g., abstract, line 1 and et seq.)

13. In the Appellant's Argument, the appellant argued (13) that applicant fails to see how the deficiency (cellular) of Paneth can be over come by Barnes. The examiner has provided no evidence from the prior art that would motivate one of ordinary skill in the art to combines Barnes with Paneth.

14. In the Appellant's Argument, the appellant argued (14) the examiner has not pointed to any teaching in the art to combine the two references. (Appellant's Brief received 12/27/02, page 18).

In response to applicant's argument (13) and (14) that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case,

Paneth does not explicitly show the use of cellular. Barnes, e.g., abstract, lines 1-4, is shown as an example that a cellular radio being well known in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a cellular radio to the system of Paneth because it would allow distribution of many of the control functions to cell stations associated with cells; thereby, monitoring and voice communication functions provides both security from interrupted service and significant reduced costs (Barnes col. 1, lines 53-63).

15. In the Appellant's Argument, the appellant argued (15) there is no teaching in either Paneth or Barnes teaches a processor that performs both management and vocoder signal processing" as required by claim 8.

In response to appellant's argument (15) that Paneth teaches wherein said first processor performs management and vocoder signal processing (e.g., fig.2, el. 24 or 17 or 20 or fig.3, el. 28 or 29; col. 7, line 63 and et seq. or col. 41, line 31).

16. In the Appellant's Argument, the appellant argued (16) there was no teaching in either Paneth or Barnes that taught the second processor is a dedicated processor adapted to bit processing as required by claim 10 (Appellant's Brief received 12/27/02. page 20.

In response to appellant's argument (16) that Paneth teaches wherein the second processor is a dedicated processor adapted to bit processing (e.g., fig.2, el. 24

or 16 or 18 or 20 or fig.3, el. 27 or 28 or 29 or fig. 25, el. 154; col. 17, line 40 and et seq).

17. In the Appellant's Argument, the appellant argued (17) Paneth and Barnes fails to teach the limitation "wherein said first, second, and third operate in parallel," as required by claim 13 (Appellant's Brief received 12/27/02. page 20).

In response to appellant's argument (17) that Paneth teaches wherein the three processors operate in parallel (e.g., abstract, line 1 and et seq).

18. In the Appellant's Argument, the appellant argued (18) Paneth and Barnes fails to teach the limitation "wherein said first processor is a digital signal processor" as required by claim 16 (Appellant's Brief received 12/27/02. page 20).

In response to appellant's argument (18) that Paneth teaches wherein the first processor is a DSP (e.g., col. 42, lines 53-60).

19. In the Appellant's Argument, the appellant argued (19) Paneth and Barnes fails to teach the limitation "wherein said first processor is a digital signal processor" as required by claim 17 (Appellant's Brief received 12/27/02. pages 21).

In response to appellant's argument (19) that Paneth teaches wherein the first processor is a DSP (e.g., col. 42, lines 53-60); wherein the second processor is a

dedicated processor adapted to bit processing (e.g., fig.2, el. 24 or 16 or 18 or 20 or fig.3, el. 27 or 28 or 29 or fig. 25, el. 154; col. 17, line 40 and et seq.).

20. In the Appellant's Argument, the appellant argued (20) there was no teaching in either Paneth or Barnes that taught the second processor is a dedicated processor adapted to bit processing as required by claim 19 (Appellant's Brief received 12/27/02. page 21.

In response to appellant's argument (20) that Paneth teaches wherein the second processor is a dedicated processor adapted to bit processing (e.g., fig.2, el. 24 or 16 or 18 or 20 or fig.3, el. 27 or 28 or 29 or fig. 25, el. 154; col. 17, line 40 and et seq.).

21. In the Appellant's Argument, the appellant argued (21) there was no teaching in either Claesson or Paneth or Barnes that suggested to one ordinary skill in the art at the time the invention to modify the first processor in Paneth to incorporate Claesson's use of a DSP to allow a highest performance, available in various forms and performance level from all major semiconductor manufacturers, to increase execution and keep the cost reasonable" (Appellant's Brief received 12/27/02. pages 22 and 24 with respect to claims 16-17).

In response to appellant's argument (21) that In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the

prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Paneth teaches the first processor performing management and vocoder signal processing (e.g., fig.2, el. 24 or 20 or fig.3, el. 29 ; col. 7, line 63 and et seq. or col. 41, line 31). Paneth does not explicitly show the above processor being a DSP. Claesson shows the use of a DSP (e.g., col. 2, page 194 to col. 1, page 195) in a radio system. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Claesson into the combines system of Paneth and Barnes because it would allow a highest performance, available in various forms and performance levels from all major semiconductor manufacturers, increase execution speed and keep the cost reasonable, as taught by Claesson(e.g., col. 2, page 194 to col. 1, page 195).

22. In the Appellant's Argument, the appellant argued (22) Paneth failed to teach processor 20 performs management and vocoder signal processing, a second processor performing protocol processing and a third processor coupled to said first processor, said third processor being a dedicated processor of the array type as required by claim 15 (Appellant's Brief received 12/27/02. pages 25-26).

In response to appellant's argument (22) that the combination of Paneth, Barns, and Mano teaches limitations of claims 15 as stated in the rejection with respect to

claim 15 above. In particular, Paneth teaches the invention substantially as claimed, a radio, comprising: a first processor performing management and vocoder signal processing (e.g., fig.2, el. 24 or 17 or 20 or fig.3, el. 28 or 29 ; col. 7, line 63 and et seq. or col. 41, line 31); a second processor coupled to the first processor wherein said second processor performs protocol processing (e.g., fig.2, el.18 or fig.3, el. 29; and col. 8, lines 22-24); a third processor coupled to the first processor wherein the third processor performs signal processing (e.g., fig.3, el. 33 or 30a or fig. 25, el. 154; col. 71, line 64 and et seq.). Paneth does not explicitly show the use of cellular. Barnes, e.g., abstract, lines 1-4, is shown as an example that a cellular radio being well known in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a cellular radio to the system of Paneth because it would allow distribution of many of the control functions to cell stations associated with cells; thereby, monitoring and voice communication functions provides both security from interrupted service and significant reduced costs. Paneth does not explicitly show the use of an array processor. Mano as an example shows that both the concept and advantages of having a processor being an array processor are well known and expected in the art (page 282). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Mano with the combined system of Paneth and Barnes because it would provide for parallel computations on large arrays, thereby increasing system computation power.

Also. Paneth teaches the processor 20 performs management and vocoder signal processing by controlling the vocoder signal processing, the interconnections between the codecs 16 (e.g., col. 8, lines 56-63).

According to col. 7, lines 60-67 and fig. 2, Paneth teaches the processor 15 (i.e., one that processes, comprising the processor 24 and converting voice information to pulse code modulation) performs management (e.g., col. 7, lines 61-63; col. 8, lines 6-64) and vocoder signal processing (e.g., col. 7, lines 63-67).

In addition, col. 41, lines 31-44 and fig. 3, el. 27 and fig. 12, Paneth teaches the processor 27 (i.e., one that processes, comprising the micropro controller 58 (fig. 12) and converting voice signal) performs management (e.g., col. 42, lines 33-40) and vocoder signal processing (e.g., col. 41, lines 30-35).

Further more, Paneth teaches the CCU processor 29 (i.e., one that processes, comprising the microprocessor 111 (fig. 21) and converting voice signal) performs management (e.g., col. 49, line 59 to col. 50, line7; col. 51, lines 29-32) and vocoder signal processing (e.g., col. 49, lines 28-60; col. 53, lines 45-50).

Paneth teaches the Voice Codec unit 28 is the processor (e.g., col. 42, lines 50-60) performs management (e.g., col. 46, lines 60 to col. 65) and vocoder signal processing (e.g., col. 8, lines 5-15).

23. In the Appellant's Argument (23), the appellant argued with respect to claims 12 and 21, there is no teaching in any of the references that would have suggested to one of ordinary skill in the art at the time of the invention to combine the three references

without the improper hindsight provided by Appellant disclosure (Appellant's Brief received 12/27/02. pages 28-29).

In response to appellant's argument (23) that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Paneth does not explicitly show the use of cellular. Barnes, e.g., abstract, lines 1-4, is shown as an example that a cellular radio being well known in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a cellular radio to the system of Paneth because it would allow distribution of many of the control functions to cell stations associated with cells; thereby, monitoring and voice communication functions provides both security from interrupted service and significant reduced costs as taught by Barns (col. 1, lines 53-63).

Paneth does not explicitly show the use of an array processor. Mano as an example shows that both the concept and advantages of having a processor being an array processor are well known and expected in the art (page 282). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Mano with the combined system of Paneth and Barnes because it would provide for

parallel computations on large arrays as taught by Mano (page 282, last paragraph), thereby increasing system computation power.

In response to applicant's argument (23) that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

24. In the Appellant's Argument, the appellant argued (24) with respect claims 12 and 21, neither reference describes itself as being applicable to large arrays (Appellant's Brief received 12/27/02. pages 28-29).

In response to appellant's argument (24) Paneth teaches the use of a plurality of processors (e.g., figs. 2-3, els. 19, 30A-30C). Mano teaches large arrays (e.g., pages 282).

25. In the Appellant's Argument, the appellant argued (25) with respect to claim 18, Paneth and Barnes fail to teach the first processor is a DSP (Appellant's Brief received 12/27/02. pages 28-29.

In response to appellant's argument (18) that Paneth teaches wherein the first processor is a DSP (e.g., col. 42, lines 53-60).

26. In the Appellant's Argument, the appellant argued (26) with respect to claim 20, Paneth and Barnes fail to teach the second processor is a dedicated processor adapted to bit processing (Appellant's Brief received 12/27/02. page 29).

In response to appellant's argument that Paneth teaches wherein the second processor is a dedicated processor adapted to bit processing (e.g., fig.2, el. 24 or 16 or 18 or 20 or fig.3, el. 27 or 28 or 29 or fig. 25, el. 154; col. 17, line 40 and et seq.).

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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